WHAT IS CLAIMED IS:

1. In a processor operating with instructions in a first instruction architecture as a native instruction, an instruction translator used with an instruction memory to store an instruction in a second instruction architecture different from said first instruction architecture, for translating an instruction in said second instruction architecture into an instruction in said first instruction architecture for application to said processor, said instruction translator comprising:

a translator for reading out an instruction from said instruction memory in response to a received first address in said instruction memory of an instruction to be executed by said processor and translating the read out instruction in said second instruction architecture into an instruction in said first instruction architecture;

an instruction cache for temporarily holding the instruction in said first instruction architecture after the translation by said translator in association with the first address in said instruction memory; and

a selector for searching said instruction cache in response to a received second address of an instruction to be executed by said processor, and for selectively outputting, based on a determination result of whether or not an instruction corresponding to the instruction of the second address is held in said instruction cache, an instruction output by said translator and the corresponding instruction held in said instruction cache.

2. The instruction translator according to claim 1, wherein said second instruction architecture is a variable length instruction architecture, and said translator includes a variable length translator for translating an instruction in said second instruction architecture read out from said instruction memory into one or more instructions in said first instruction architecture, the number of which depends on an instruction length of the read out instruction in said second instruction architecture.

3. The instruction translator according to claim 2, wherein said

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variable length translator translates the instruction in said second instruction architecture read out from said instruction memory into an instruction in said first instruction architecture depending on the instruction length of said read out instruction in said second instruction architecture and having a length larger than the instruction length.

4. The instruction translator according to claim 3, wherein each instruction in said first instruction architecture includes one or a plurality of sub instructions, and the number of the sub instructions included in the instruction in the first instruction architecture translated by said variable length translator depends on the instruction length of said read out instruction in said second instruction architecture.

5. The instruction translator according to claim 1, wherein said translator includes a plurality of translators which translate a plurality of instructions in said second instruction architecture read out from said instruction memory into one instruction in said first instruction architecture.

6. The instruction translator according to claim 1, wherein each instruction in said first instruction architecture can include one or a plurality of sub instructions, and

said translator translates a plurality of instructions in said second instruction architecture read out from said instruction memory into an instruction in said first instruction architecture including sub instructions, the number of which depends on the number of said plurality of instructions.

7. The instruction translator according to claim 6, wherein the number of sub instructions included in the instruction in said first instruction architecture after said translation is equal to the number of said plurality of instructions.

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8. The instruction translator according to claim 1, wherein said translator translates said read out instruction in said second instruction architecture into one or a plurality of instructions as the instruction in said first instruction architecture;

said instruction translator further comprises a controller for controlling said instruction cache so that said instruction cache holds each of said one or said plurality of instructions held in said instruction cache as an entry which can be invalidated in one of first and second conditions.

9. The instruction translator according to claim 8, wherein said first condition is a holding control condition by hardware control based on a prescribed algorithm by said instruction cache, and

said second condition is a condition in which an explicit invalidation instruction is applied from the outside of said instruction cache.

10. The instruction translator according to claim 8, wherein said controller outputs a signal asserted when a new instruction cannot be held in said instruction cache without invalidating an entry which can be invalidated in the second condition.

11. The instruction translator according to claim 8, wherein said translator translates the read out instruction in said second instruction architecture into the plurality of instructions as the instruction in said first instruction architecture, and said controller provides said first condition with one of said plurality of instructions and said second condition with each of said plurality of instruction but said one instruction.

12. An instruction memory attached with a translator, used with a processor operating with an instruction in a first instruction architecture as a native instruction, comprising:

an instruction storage unit to store an instruction in a second instruction architecture; and

an instruction translator to translate an instruction in said second

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instruction architecture output from said instruction storage unit into an instruction in said first instruction architecture for application to said processor.

13. The instruction memory attached with a translator according to claim 12, wherein said instruction translator includes a selector to select one of the processing to translate the instruction in said second instruction architecture into the instruction in said first instruction architecture and the processing of outputting the instruction in said second instruction architecture as it is, based on an address of an instruction to be executed which is read out from said instruction storage unit.

14. The instruction memory attached with a translator according to claim 12, further comprising an address translator to translate an address at the time of reading from said instruction storage unit.

15. The instruction memory attached with a translator according to claim 12, wherein said instruction translator includes:

a translator to read out the instruction in said second instruction architecture from said instruction storage unit in response to a received first address of an instruction to be executed by said processor and translate the read out instruction in said second instruction architecture into the instruction in said first instruction architecture;

an instruction cache to temporarily hold the instruction in said first instruction architecture after the translation by said translator in association with the first address; and

a selector to search said instruction cache in response to a received second address of an instruction to be executed by said processor and selectively output to said processor, based on a determination result of whether or not an instruction corresponding to the instruction of the address is held in said instruction cache, an instruction output by said translator and the corresponding instruction in said first instruction architecture held in said instruction cache.

16. A data processing apparatus, comprising:

a processor operating with an instruction in a first instruction architecture as a native instruction;

a bus to which said processor is connected; and

an instruction memory with a translator interconnected with said processor through said bus,

said instruction memory with a translator including:

an instruction storage unit to store an instruction in a second instruction architecture transferred from said processor through said bus; and

an instruction translator to translate the instruction in said second instruction architecture output from said instruction storage unit into an instruction in said first instruction architecture for application to said processor through said bus.

17. The data processing apparatus according to claim 16, further comprising, a second instruction memory interconnected to said processor through said bus, said second instruction memory including:

an instruction storage unit to store an instruction in said first instruction architecture transferred from said processor through said bus; and

an instruction reading circuit responsive to an address signal applied from said processor through said bus for applying an instruction in said first instruction architecture output from said instruction storage unit to said processor through said bus.

18. The data processing apparatus according to claim 15, wherein the wait number of said bus when an instruction read out from said instruction memory with a translator is transferred to said processor is controlled to be larger than the wait number of said bus when an instruction read out from said second instruction memory is transferred to said processor.

19. The data processing apparatus according to claim 18, further comprising a third instruction memory with a translator interconnected to said processor through said bus,

said third instruction memory with a translator including:

an instruction storage unit to store an instruction in a third instruction architecture different from said second instruction architecture, said instruction in said third instruction architecture being transferred from said processor through said bus; and

an instruction translation circuit responsive to an address signal applied from said processor through said bus, for translating an instruction in said third instruction architecture output from said instruction storage into an instruction in said first instruction architecture for application to said processor.